REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the present application.

The Examiner's final Office Action dated August 13, 2001 has been received and its contents carefully noted. Claims 1-47 were pending in the present application. By this amendment, claims 1, 7, 8, 14, 15, 21, 23, 29-31, 36 and 42 have been amended and new claims 48-52 have been added. Accordingly, claims 1-52 are now pending, of which claims 1, 8, 15, 23, 31, 36, 42 and 48 are independent.

Claims 1, 2, 4, 6-9, 11, 13-16, 18, 20-24, 26 and 28-30 are Not Anticipated by Zhang

Claims 1, 2, 4, 6-9, 11, 13-16, 18, 20-24, 26 and 28-30 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Zhang et al., U.S. Patent No. 5,424,244 (Zhang).

The Examiner is reminded that in order to form a proper anticipation rejection under 35 U.S.C. § 102, the reference must disclose each and every element of the claimed invention. *See* M.P.E.P. § 2131; *Verdegaal Bros. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991); *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997); *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 1047 (Fed. Cir. 1995). Specifically, two conditions must be met as follows: (1) all the elements of the claim must be properly construed, and (2) all the elements of the claim, as properly construed, must be disclosed in the prior art reference either explicitly or inherently. *Elmer v. ICC Fabricating, Inc.*, 67 F.3d 1571, 1574 (Fed. Cir. 1995); *Schreiber*, 128 F.3d at 1477; *Glaxo*, 52 F.3d at 1047.

With respect to independent claims 1, 8, 15, and 23, Zhang fails to teach the claimed limitation of the first insulating film formed over the insulating surface, the semiconductor layer, the gate insulating film and the gate electrode. The Examiner contends in the Office Action that a reference numeral 209 in Zhang denotes the first insulating film. However, 209 denotes a drain as described in the last line of column 16. It appears that Fig. 11(B) of Zhang has been mislabeled. Reference numeral 209 in Fig. 11(B) should be an anodically oxidized product 207 as shown in col. 16, lines 61-64. Nonetheless, the anodically oxidized product 207 of Zhang is not the same as the first insulating film of the present invention. Specifically, the anodically

oxidized product 207 is not formed over the insulating surface, the semiconductor layer, the gate insulating film and the gate electrode. In contrast, the anodically oxidized product 207 only covers the aluminum gate electrode 206. (See Fig. 2F of the present invention and compare to Fig. 11(E) of Zhang.) The Examiner has not properly construed the claims, and the reference does not disclose all of the elements of the claim either explicitly or inherently. The Applicants respectfully request that the claim rejection under 35 U.S.C. § 102(e) be withdrawn and that the claims should be held allowable.

Claims 1-4, 6-11, 13-18, 20-26 and 28-30 are Patentable Over Hsieh and Tran

Claims 1-4, 6-11, 13-18, 20-26 and 28-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsieh, U.S. Patent No. 5,153,142 (Hsieh) in view of Tran et al., U.S. Patent No. 5,273,910, (Tran).

It should be noted that three criteria must be met to establish a prima facie case of obviousness. *M.P.E.P. § 2143.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to achieve the claimed invention. *Id.* Second, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). Third, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

The Applicants respectfully contend that the Examiner has failed to set forth a *prima facie* case of obviousness. First, the Examiner has not given any indication that one with ordinary skill in the art at the time of the invention would have had a reasonable expectation of success when combining Hsieh and Tran.

Furthermore, the prior art does not teach or suggest all the claim limitations. The independent claims recite a pixel electrode formed over the second insulating film comprising an organic resin formed on the first insulating film. The Applicants respectfully submit that the claimed limitation cannot be obtained even if Hsieh and Tran are combined, because neither Hsieh nor Tran teaches the pixel electrode formed over the second insulating film comprising an organic resin formed on the first insulating film.

The Applicants further contend that even assuming, *arguendo*, that the combination of Hsieh and Tran is proper, there is a lack of suggestion as to why a skilled artisan would use the

proposed modifications to achieve the unobvious advantages first recognized by the Applicants. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990).

Claims 5, 12, 19, 27 and 31-47 are Patentable Over Hseih, Tran and Liauh

Claims 5, 12, 19, 27 and 31-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsieh in view of Tran and further in view of Liauh, U.S. Patent No. 5,027,185 (Liauh).

Please incorporate by reference the arguments made with respect to claims 1-4, 6-11, 13-18, 20-26 and 28-30 above.

Liauh does not correct the deficiencies in Hsieh and Tran. The Examiner cites Liauh in order to teach first and second conductive films (p. 6, Paper No. 6). Neither Hseih and Tran, nor Hseih and Tran in view of Liauh teaches or suggests a pixel electrode formed over the second insulating film comprising an organic resin formed on the first insulating film. The Applicants respectfully submit that the claim rejections under 35 U.S.C. §§ 102(e) and 103(a) should be withdrawn, and all the rejected claims should be allowable.

New Claims 48-52 are Patentable

New claims 48-52 have been introduced to better claim the features of the invention. Support for the claims can be found in Fig. 2F an in the specification at page 22.

Conclusion

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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Attachments

MARKED-UP VERSION
OF THE AMENDED CLAIMS

1. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel [formation] region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed [on] over said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed [on] over said second insulating film.

7. (Amended) A semiconductor device of claim 1 wherein a portion of said pixel electrode is located under said electrode.

8. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel [formation] region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed [on] over said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed [on] over said second insulating film.

14. (Amended) A semiconductor device of claim 8 wherein a portion of said pixel electrode is located under said electrode.

15. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel [formation] region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed [on] over said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed [on] over said second insulating film.

21. (Amended) A semiconductor device of claim 15 wherein a portion of said pixel electrode is located under said electrode.

23. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel [formation] region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed [on] over said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed [on] over said second insulating film.

29. (Amended) A semiconductor device of claim 23 wherein a portion of said pixel electrode is located under said electrode.

30. (Amended) A semiconductor device of claim 23 wherein said transparent pixel electrode comprises indium tin oxide.

31. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel [formation] region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed [on] over said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a pixel electrode formed [on] over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode [wherein said second conductive film is interposed between said pixel electrode and said first conductive film]; and

a conductive layer formed [on] over said second insulating film and connected to the other one of said first and second impurity regions.

36. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel [formation] region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed [on] over said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate structure including a first

conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed [on] over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode [wherein said second conductive film is interposed between said pixel electrode and said first conductive film]; and

a conductive layer formed [on] over said second insulating film and connected to the other one of said first and second impurity regions.

42. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel [formation] region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed [on] over said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed [on] over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode [wherein said second conductive film is in direct contact with said one of the impurity regions and said transparent pixel electrode and said first conductive film is formed on said second conductive film]; and

a conductive layer formed [on] over said second insulating film and connected to the other one of said first and second impurity regions, wherein said electrode comprises a same material as said conductive layer.